WHAT IS CLAIMED IS:

1. An image display apparatus comprising:

a plurality of scan wirings;

a plurality of modulation wirings for constituting a matrix wiring together with the scan wirings;

display elements to be driven in matrix according to a scan signal applied by the scan wirings and a modulation signal applied by the modulation wirings;

a scan circuit for selecting the plurality of scan wirings one after another and applying a scan signal to the selected scan wiring;

an output circuit for storing an input signal to be inputted in time-series, generating a plurality of outputs consisting of a time-series signal for generating a modulation signal based on the stored result and outputting the plurality of outputs to a plurality of output paths as parallel outputs; and

a modulation side drive circuit for outputting parallel modulation signals based on the time-series signal for generating a modulation signal,

wherein the modulation side drive circuit is provided in a plural form corresponding to each of the plurality of output paths and each of the plurality of modulation side drive circuits supplies the modulation signal to a part of and a plurality of

modulation wirings among the plurality of modulation wirings, and

wherein the output circuit starts to output at least one of the parallel outputs before storing the input signal for constituting the rearmost end among respective rear ends of the parallel outputs.

2. An image display apparatus according to claim 1, wherein a plurality of outputs among the parallel outputs are started to be outputted substantially simultaneously.

3. An image display apparatus according to claim 1, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and starts to output a first output corresponding to the first part when a Dth output corresponding to the Dth part is ready to be outputted or later.

4. An image display apparatus according to claim 2, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the

output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and starts to output a first output corresponding to the first part when a Dth output corresponding to the Dth part is ready to be outputted or later.

5. An image display apparatus according to claim 3, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts, and starts to output a first output corresponding to the first part substantially simultaneously with the start of output of a Dth output corresponding to the Dth part.

6. An image display apparatus according to claim 4, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts, and starts to output a first output corresponding to the first part substantially simultaneously with the start of output of a Dth output corresponding to the

Dth part.

7. An image display apparatus according to claim 5, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and starts to output the D outputs substantially simultaneously.

8. An image display apparatus according to claim 6, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and starts to output the D outputs substantially simultaneously.

9. An image display apparatus according to claim 1, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs

substantially simultaneously.

10. An image display apparatus according to claim 2, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs substantially simultaneously.

11. An image display apparatus according to claim 3, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs substantially simultaneously.

12. An image display apparatus according to claim 4, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs

substantially simultaneously.

13. An image display apparatus according to claim 5, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs substantially simultaneously.

14. An image display apparatus according to claim 6, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs substantially simultaneously.

15. An image display apparatus according to claim 7, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs

substantially simultaneously.

16. An image display apparatus according to claim 8, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, and the output circuit is for outputting the D parallel outputs based on each of the D parts and finishes outputting the D outputs substantially simultaneously.

17. An image display apparatus according to any one of claims 1 to 16, wherein an input signal to be inputted in the output circuit in time-series in order to output the plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied in parallel with each other to the modulation wirings, the output circuit is for storing the n time-series input signals in first to Dth memories (D is an integer equal to or larger than 2) one after another in the order of input, and each of the memories is for writing the input signal in an address designated by a write address to be given and reading a signal written in an address designated by a read address to be given,

wherein a write address to be given to an Xth

memory ($1 \leq X \leq D$) changes during a period from the time when an $n(X-1)/D+1$th input signal among the n input signals is inputted until the time when nX/Dth input signal is inputted in the order of 1 to n/D in synchronism with the input signals, and

wherein the signal stored in each of the memories is read out by giving the read address to each memory and an output from each memory is outputted as the D parallel outputs.

18. An image display apparatus according to claim 17, wherein the read address to be given to the Xth memory ($1 \leq X \leq D$) changes during a period from the time when $n(D-1)/D+1$th input signal among the n input signals is inputted until the time when n/Dth input signal among the next n input signals is inputted in the order of 1 to n/D.

19. An image display apparatus according to claim 18, wherein the read address to be given to the Xth memory ($1 \leq X \leq D$) changes using an entire period from the time when $n(D-1)/D+1$th input signal among the n input signals is inputted until the time when n/Dth input signal among the next n input signals is inputted in the order of 1 to n/D.

20. An image display apparatus according to

claim 1, further comprising a delay circuit, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts and starting to output at least one output among the D outputs earlier than starting to output other outputs, and the delay circuit is for delaying inputting the output which is started to be outputted earlier in the modulation side drive circuit.

21. An image display apparatus according to claim 1, further comprising a delay circuit, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 3) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts and starts to output each of first to D-2th outputs corresponding to the first to D-2th parts, respectively, earlier than output of D-1th part and Dth part, and the delay circuit is for delaying inputting each of the first to D-2th outputs in each of the modulation side drive circuits.

22. An image display apparatus according to

claim 1, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 3) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts and starting an Xth output ($1 \leq X \leq D-1$) at a delay of a first predetermined period from the start of input of the first part and starting a Dth output at a delay of a second predetermined period from the start of input of the first part, where the first predetermined period is X/D of a reference period that is a period required for inputting the first to Dth parts and the second predetermined period is (D-1)/D of the reference period, and

wherein a delay circuit for giving a delay to an Xth output ($1 \leq X \leq D-2$) is further provided and a delay amount by the delay circuit is (D-X-1)/D of the reference period.

23. An image display apparatus according to claim 1 or any one of claims 20 to 22, wherein the input signal to be inputted in the output circuit in time-series in order to output the plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied in parallel with each other to the modulation wirings, the output circuit is for storing the n time-series

input signals in first to Dth memories (D is an integer equal to or larger than 3) one after another in the order of input, and each of the memories is for writing the input signals in an address designated by a write address to be given and reading an signal written in an address designated by a read address to be given,

wherein a write address to be given to an Xth memory ($1 \leq X \leq D$) changes during a period from the time when an $n(X-1)/D+1$th input signal among the n input signals is inputted until the time when nX/Dth input signal is inputted in the order of 1 to n/D in synchronism with the input signals,

wherein the read address to be given to the Xth memory ($1 \leq X \leq D-1$) changes during a period from the time when $nX/D+1$th input signal among the n input signals is inputted until the time when nX/Dth input signal among the next n input signals is inputted in the order of 1 to n/D,

wherein a read address to be given to the Dth memory changes in the same manner as a read address to be given to a D-1th memory, and

wherein an output from each memory is outputted as the D parallel outputs.

24. An image display apparatus according to claim 23, wherein the input signal to be inputted in

the output circuit in time-series in order to output the plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied to the modulation wirings in parallel, the output circuit is for storing the n time-series input signals in first to Dth memories (D is an integer equal to or larger than 3) one after another in the order of input, and each of the memories is for writing the input signals in an address to be designated by a write address to be given and reading a signal written in an address designated by a read address to be given,

wherein a write address to be given to an Xth memory ($1 \leq X \leq D$) changes during a period from the time when an $n(X-1)/D+1$th input signal among the n input signals is inputted until the time when nX/Dth input signal is inputted in the order of 1 to n/D in synchronism with the input signals,

wherein the read address to be given to the Xth memory ($1 \leq X \leq D-1$) changes using an entire period from the time when $nX/D+1$th input signal among the n input signals is inputted until the time when nX/Dth input signal among the next n input signals is inputted in the order of 1 to n/D,

wherein a read address to be given to the Dth memory changes in the same manner as a read address to be given to a D-1th memory, and

wherein an output from each memory is outputted as the D parallel outputs.

25. An image display apparatus according to claim 1, wherein the plurality of modulation side drive circuits are for supplying modulation signals to the same number of the modulation wirings, respectively.

26. An image display apparatus according to any one of claims 1 to 8, wherein the number of modulation wirings to which each of the plurality of modulation side drive circuits supplies a modulation signal is not the same number.

27. An image display apparatus according to claim 26, wherein: the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit; the output circuit is for outputting the D parallel outputs based on each of the D parts; and the number of modulation wirings to which the modulation side drive circuit, in which a first output corresponding to the first part is inputted, supplies a modulation signal is fewer than the number of modulation wirings to which the modulation side drive circuit, in which a Dth output corresponding to

the Dth part is inputted, supplies a modulation signal.

28. An image display apparatus according to claim 26, wherein the input signal to be inputted in time-series in the output circuit in order to output the plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied in parallel with each other to the modulation wirings and satisfies a condition:

$$d[X] \leqq M\left(d[D] + \sum_{x=1}^{X} d[x]\right) \quad [X = 1 \sim D-1]$$

$$d[D] \leqq M\left(\sum_{x=1}^{D} d[x]\right)$$

$$\cdots \quad (1)$$

when the output circuit turns the n time-series input signals into first to Dth parts (D is an integer equal to or larger than 2) in the order of input and outputs an output corresponding to each part as the plurality of parallel outputs, a ratio of the number of modulation wirings to which the modulation side drive circuit, in which an output corresponding to each part is inputted, supplies the modulation signal is d[1]:d[2]:...:d[D-1]:d[D], and a transfer speed of

a signal in each of the output paths is a speed M times as large as the input speed of the input signal.

29. An image display apparatus according to claim 26, wherein the input signal to be inputted in time-series in the output circuit in order to output the plurality of parallel outputs is n time-series input signals for generating n modulation signals to be supplied in parallel with each other to the modulation wirings and satisfies a condition:

$$d[X] = M\left(d[D] + \sum_{x=1}^{X} d[x] \right) \quad [X = 1 \sim D-1]$$

$$d[D] = M\left(\sum_{x=1}^{D} d[x] \right)$$

$$\cdots \quad (2)$$

when the output circuit turns the n time-series input signals into first to Dth parts (D is an integer equal to or larger than 2) in the order of input and outputs an output corresponding to each part as the plurality of parallel outputs, a ratio of the number of modulation wirings to which the modulation side drive circuit, in which an output corresponding to each part is inputted, supplies the modulation signal is d[1]:d[2]:...:d[D-1]:d[D], and a transfer speed of

a signal in each of the output paths is a speed M times as large as the input speed of the input signal.

30. An image display apparatus according to claim 1, wherein the output circuit has a memory for carrying out the storage and a memory for storing at least the Dth part is a memory capable of nonexclusively carrying out writing and reading.

31. An image display apparatus according to claim 30, wherein the memory for storing the first part is a memory capable of nonexclusively carrying out writing and reading.

32. An image display apparatus according to claim 1, wherein: the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit; the output circuit is for outputting the D parallel outputs based on each of the D parts; memories are provided corresponding to each of the D output paths for outputting the D outputs; at least one of the D memories has two memory blocks for nonexclusively carrying out writing and reading; and after a part of corresponding parts among the D parts is written in one memory block, the two memory blocks carry out writing of the subsequent part in the other

memory block and reading of a signal from the memory block in which a part of the input signal is written previously while causing at least a part of the writing and reading to overlap each other.

33. An image display apparatus according to claim 32, wherein each of the D memories has the two memory blocks.

34. An image display apparatus according to claim 32, in which one of the parallel outputs is constituted by signals read out from each of the two memory blocks one after another, the apparatus further comprising a delay circuit for alleviating deviation in starting of input of each of the parallel outputs in each of the modulation side drive circuits.

35. An image display apparatus according to claim 33, in which one of the parallel outputs is constituted by signals read out from each of the two memory blocks one after another, the apparatus further comprising a delay circuit for alleviating deviation in starting of input of each of the parallel outputs in each of the modulation side drive circuits.

36. An image display apparatus according to claim 32, wherein when numbers are allocated to memory blocks, which are provided two for each of the first to Dth outputs, in the order of inputting the input signals, the number of input signals to be written in a memory block of an odd number and the number of input signals to be written in a memory block of an even number satisfy the following expression:

$1/D \leq$ the number of input signals to be written in a memory block of an odd number/the number of input signals to be written in a memory block of an even number $\leq D$, and

wherein the number of input signals to be written in each memory block is equal to or more than $1/D(D+1)$ times and equal to or less than $D/D(D+1)$ times the total number of modulation wirings through which each modulation side drive circuit supplies a modulation signal.

37. An image display apparatus according to claim 33, wherein when numbers are allocated to memory blocks, which are provided two for each of the first to Dth outputs, in the order of inputting the input signals, the number of input signals to be written in a memory block of an odd number and the number of input signals to be written in a memory

block of an even number satisfy the following expression:

1/D ≤ the number of input signals to be written in a memory block of an odd number/the number of input signals to be written in a memory block of an even number ≤ D, and

wherein the number of input signals to be written in each memory block is equal to or more than 1/D(D+1) times and equal to or less than D/D(D+1) times the total number of modulation wirings through which each modulation side drive circuit supplies a modulation signal.

38. An image display apparatus according to claim 34, wherein when numbers are allocated to memory blocks, which are provided two for each of the first to Dth outputs, in the order of inputting the input signals, the number of input signals to be written in a memory block of an odd number and the number of input signals to be written in a memory block of an even number satisfy the following expression:

1/D ≤ the number of input signals to be written in a memory block of an odd number/the number of input signals to be written in a memory block of an even number ≤ D, and

wherein the number of input signals to be

written in each memory block is equal to or more than 1/D(D+1) times and equal to or less than D/D(D+1) times the total number of modulation wirings through which each modulation side drive circuit supplies a modulation signal.

39. An image display apparatus according to claim 35, wherein when numbers are allocated to memory blocks, which are provided two for each of the first to Dth outputs, in the order of inputting the input signals, the number of input signals to be written in a memory block of an odd number and the number of input signals to be written in a memory block of an even number satisfy the following expression:

1/D ≤ the number of input signals to be written in a memory block of an odd number/the number of input signals to be written in a memory block of an even number ≤ D, and

wherein the number of input signals to be written in each memory block is equal to or more than 1/D(D+1) times and equal to or less than D/D(D+1) times the total number of modulation wirings through which each modulation side drive circuit supplies a modulation signal.

40. An image display apparatus according to

any one of claims 32 to 39, wherein when numbers are allocated to memory blocks, which are provided two for each of the first to Dth outputs, in the order of inputting the input signals,

if X is an odd number from 1 to 2D-3 and 2D, the number of input signals to be written in an Xth memory block is D/D(D+1) times the total number of modulation wirings to which each modulation side drive circuit supplies a modulation signal, and

if X is an even number from 2 to 2D-2 and 2D-1, the number of input signals to be written in an Xth memory block is 1/D(D+1)times the total number of modulation wirings to which each modulation side drive circuit supplies a modulation signal.

41. An image display apparatus according to claim 1, wherein transfer speeds of the plurality of parallel outputs are substantially equal.

42. An image display apparatus according to claim 1, wherein the signal to be inputted in time-series has first to Dth parts (D is an integer equal to or larger than 2) in the order of input in the output circuit, the output circuit is for outputting the D parallel outputs based on each of the D parts, and the D parallel outputs are started to be inputted in each of the modulation side drive circuits

substantially simultaneously.

43. An image display apparatus according to claim 1, in which an R input signal, a G input signal and a B input signal are inputted respectively, and the output circuits are provided for the input signals of each color, the apparatus further comprising a composition circuit for composing outputs to be outputted to the same modulation side drive circuit among the plurality of parallel outputs of each output circuit.

44. An image display apparatus according to claim 1, wherein the display element is an electron-emitting element.

45. An image display apparatus comprising:

a plurality of scan wirings;

a plurality of modulation wirings constituting a matrix wiring together with the scan wirings;

display elements driven in matrix according to a scan signal to be applied by the scan wirings and a modulation signal applied by the modulation wirings;

a scan circuit for selecting the plurality of scan wirings one after another and applying a scan signal to the selected scan wiring;

an output circuit including a first output

circuit for storing an input signal for displaying a first color to be inputted in time-series and generating D outputs (D is an integer equal to or larger than 2) consisting of time-series signals for generating modulation signals based on the stored result to output the D outputs to D output paths as parallel outputs, a second output circuit for storing an input signal for displaying a second color to be inputted in time-series and generating D outputs consisting of time-series signals for generating modulation signals based on the stored result to output the D outputs to D output paths as parallel outputs, and D composition circuits for composing outputs that are outputted to an Xth output path ($1 \leq X \leq D$) among the D output paths to which the outputs from the first output circuit are outputted and an Xth output path ($1 \leq X \leq D$) among the D output paths to which the outputs from the second output circuit are outputted respectively; and

a modulation side drive circuit for outputting parallel modulation signals based on time-series signals for generating modulation signals to be outputted from the composition circuit,

wherein the modulation side drive circuit is provided in plural forms associated with each of the D composition circuits and each of the plurality of modulation side drive circuits supplies the

modulation signal to a part of and a plurality of modulation wirings among the plurality of modulation wirings,

wherein the display elements are arranged such that a plurality of display elements to which the scan signals are given simultaneously by one scan wiring include a display element for displaying the first color and a display element for the second color, and

wherein the composition circuit is for composing outputs from the first output circuit and the second output circuit according to the arrangement of the display element for displaying the first color and the display element for displaying the second color.

46. An image display apparatus comprising:

a plurality of scan wirings;

a plurality of modulation wirings constituting a matrix wiring together with the scan wirings;

display elements to be driven in matrix according to a scan signal applied by the scan wirings and a modulation signal applied by the modulation wirings;

a scan circuit for selecting the plurality of scan wirings one after another and applying a scan signal to the selected scan wiring;

an output circuit including a first output circuit for storing an input signal for displaying red to be inputted in time-series and generating D outputs (D is an integer equal to or larger than 2) consisting of time-series signals for generating modulation signals based on the stored result to output the D outputs to D output paths as parallel outputs, a second output circuit for storing an input signal for displaying green to be inputted in time-series and generating D outputs consisting of time-series signals for generating modulation signals based on the stored result to output the D outputs to D output paths as parallel outputs, a third output circuit for storing an input signal for displaying blue to be inputted in time-series and generating D outputs consisting of time-series signals for generating modulation signals based on the stored result to output the D outputs to D output paths as parallel outputs, and D composition circuits for composing outputs that are outputted to an Xth output path ($1 \leq X \leq D$) among the D output paths to which the outputs from the first output circuit are outputted, an Xth output path ($1 \leq X \leq D$) among the D output paths to which the outputs from the second output circuit are outputted, and an Xth output path ($1 \leq X \leq D$) among the D output paths to which the outputs from the third output circuit are outputted respectively; and

a modulation side drive circuit for outputting parallel modulation signals based on time-series signals for generating modulation signals to be outputted from the composition circuit,

wherein the modulation side drive circuit is provided in plural forms associated with each of the D composition circuits and each of the plurality of modulation side drive circuits supplies the modulation signal to a part of and a plurality of modulation wirings among the plurality of modulation wirings,

wherein the display elements are arranged such that a plurality of display elements to which the scan signals are given simultaneously by one scan wiring include a display element for displaying red, a display element for displaying green and a display element for displaying blue, and

wherein the composition circuit is for composing outputs from the first output circuit, the second output circuit and the third output circuit according to the arrangement of the display element for displaying red, the display element for displaying green and the display element for displaying blue.